Code No: 9A10504/R09

B.Tech. III Year II Semester Regular & Supplementary Examinations

Set-3

April/May - 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 Hours | Max. Marks: 70

*Answer any **FIVE** Questions*

*All Questions carry **Equal** Marks*

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1.	(a)	Give the design procedure of a compensating network for an OP- AMP which uses ± 10 V supply voltages. Assume necessary data.	
	(b)	Explain A.C analysis of differential amplifier.	
2.	(a)	Describe the principle of operation of precision half-wave rectifier with waveforms.	
	(b)	Explain the operation of antilog amplifier using op-amp.	
3.	(a)	Explain how a 555 timer in astable mode can be used for FSK generation.	
	(b)	Design a PLL circuit using 565 IC to get free running frequency = 4.5 kHz, lock range = 2 kHz, capture range = 100 Hz. Assume supply voltages of ± 10 V are available. Show the circuit diagram.	
4.	(a)	What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values for a CMOS NAND gate.	
	(b)	Compare HC, HCT, VHC and VHCT CMOS logic families with the help of output specifications with V_{CC} from 4.5 to 5.5 V.	
5.	(a)	Explain the features of the TTL logic family.	
	(b)	Explain the concept and implementation of ECL logic family.	
6.	(a)	Explain the various data types supported by VHDL. Give the necessary examples.	
	(b)	Write a VHDL program to detect prime number of a 8-bit input.	
7.	(a)	Design a 24-bit group ripple adder using 74 × 283 ICs.	
	(b)	Explain de-multiplexer in detail.	
8.	(a)	Design an 8-bit synchronous binary counter with serial enable control.	
	(b)	Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table.	